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Abstract
In a digital signal processor, the multiplier plays a major role in the processor not only for the circuit delay but also for the power consumption. There are many kinds of multipliers; array multipliers are very popular due to property of regular structure. However, array multipliers may consume more power when the glitch effect exists in the circuit.
In the thesis, we have proposed a new design method of hybrid left to right array multiplier to reduce the glitch effect and the switching activities. The new multiplier combines the properties of the leapfrog and split multipliers to the glitches in the circuit and then the power consumption can be reduced. The new multiplier also adopts the dynamic range detection method to lower switching activities during the addition of partial products. We have implemented the new multiplier by using the cell-based design method with a TSMC 0.35μm cell library. The experimental results show that our new multiplier has the advantages of low power and high speed properties.
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